16. The method of claim **15**, further comprising comparing one or more delayed versions of the first signal, each delayed version of the first signal delayed based on the clock signal, the frequency low signal based on one or more of the delayed versions of the first signal.

17. The method of claim **16**, further comprising detecting a division.

18. The method of claim **12**, further comprising outputting a frequency high signal based on the second signal.

19. The method of claim **18**, further comprising comparing one or more delayed versions of the second signal to generate the frequency high signal, the frequency high signal based on the comparison of one or more delayed versions of the second signal, each delayed version of the second signal delayed based on the clock signal.

20. The method of claim **19**, further comprising:

doubling the frequency of the clock signal;

comparing the clock signal period of the doubled clock signal to the delay period;

outputting the first signal, wherein the period of the first signal is double the doubled clock signal period when the doubled clock signal period is greater than the delay period; and

outputting the second signal, wherein the period of the second signal is greater than double the doubled clock signal period when the doubled clock signal period is less than the delay period.

21. An apparatus for detecting an incorrect clock frequency, the apparatus comprising:

means for comparing a clock signal period to a delay period;

means for outputting a first signal, wherein the period of the first signal is double the clock signal period when the clock signal period is greater than the delay period; and

means for outputting a second signal, wherein the period of the second signal is greater than double the clock signal period when the clock signal period is less than the delay period.

22. The apparatus of claim **21**, means for outputting, on a single output, the first signal when the clock signal period is greater than the delay period and outputting, on the single output, the second signal when the clock signal period is less than the delay period.

23. The apparatus of claim **22**, wherein the first signal is output when the clock signal period is equal to the delay period.

24. The apparatus of claim **21**, further comprising means for outputting a frequency low signal based on the first signal.

25. The apparatus of claim **24**, further comprising means for comparing one or more delayed versions of the first signal, each delayed version of the first signal delayed based on the clock signal, the frequency low signal based on one or more of the delayed versions of the first signal.

26. The apparatus of claim **25**, further comprising means for detecting a division ratio.

27. The apparatus of claim **21**, further comprising means for outputting a frequency high signal based on the second signal.

28. The apparatus of claim **27**, further comprising means for comparing one or more delayed versions of the second signal to generate the frequency high signal, the frequency high signal based on the comparison of one or more delayed versions of the second signal, each delayed version of the second signal delayed based on the clock signal.

29. The apparatus of claim **28**, further comprising:

means for doubling the frequency of the clock signal;

means for comparing the clock signal period of the doubled clock signal to the delay period;

means for outputting the first signal, wherein the period of the first signal is double the doubled clock signal period when the doubled clock signal period is greater than the delay period; and

means for outputting the second signal, wherein the period of the second signal is greater than double the doubled clock signal period when the doubled clock signal period is less than the delay period.

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